IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Teterud	Docket No:	TI-32304
Serial No:	10/044,678	Examiner:	Patel, Ishwarbhai B.
Filed:	1/11/2002	Art Unit:	2827

For: PREAMP PINOUT TO ACCOMMODATE MULTIPLE R/W HEAD STYLES FOR FLIP CHIP HDD SYSTEMS

APPEAL BRIEF PURSUANT TO 1.192(c)

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on 5-21-04.

Tommie Chambers

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the final Office Action mailed November 6, 2003, and the Advisory Action mailed March 19, 2004.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-6 originally filed, and no claims were cancelled. Thus, the subject matter of the instant appeal is the final rejection of Claims 1-6.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-6. A Response was filed on July 11, 2003, canceling no claims. Additionally, a Response was filed on February 5, 2004 again canceling no claims.

The Advisory Action indicated that the Response of February 5, 2004 had been considered.

SUMMARY OF THE INVENTION

Figures 7 and 8 show a side and top view, respectively, of the disk drive system designated by the general reference 1100 within an enclosure 1110.

An AE module 1194 mounted on the connection circuit 1193 of the present invention or carrier that comprises circuitry preferably implemented in an integrated circuit (IC) chip including read drivers, write drivers, and associated control circuitry.

Turning now to Figure 2, three possible head styles with their associated pin locationon the "flex", which connects and interfaces to the physical heads, are illustrated with their four heads named: WX, WY, RY and RX. First head style 202 has connection point 230 for signal WX, connection point 232 for signal WY, connection point 234 for signal RX and connection point 236 for signal RY.

Connection style 204 has connection point 220 for signal RX, connection point 222 for signal RY, connection point 224 for signal WX and connection point 226 for signal WY.

The third style 206 has connection point 210 for signal WX, connection point 212 for signal WY, connection point 214 for RY and connection point 216 for signal RX.

Figure 4 illustrates a connection circuit with element 410, which includes the connection points for two channels, element 412 which includes the connection points for another two channels, and element 414 which includes connection points for four additional channels illustrating a total of eight channels. Elements 410 and 412 could be left unconnected, being connected for a four-channel device. Element 410 could be unconnected, being connected for a six-channel device. Using element 414 as representative of all elements 410, 412 and 414, element 414 includes an outside row 420 and inside row 422 of connection points for the head. As illustrated in Figure 4, the connection points for the read signals are in the outside row 420 and the connection points for the write signals are on the inside row 422. Element 402 collectively illustrates control signals that are used for the preamp chip. Additionally, element 404 and element 406 control voltages such as ground and system supply.

Figure 5 illustrates the connection chip for connection with style 204. This signal routing option is possible due to achieving appropriate spacing requirements.

Turning now to Figure 6, style 206 has been implemented. By using inner and outer rows, a connection chip can be constructed to accommodate either eight-channel or four-channel without a redesign of the metals or layers.

Figure 3 illustrates a preamp chip having input power supply signals G, E and C. Thus, with multiple connection points, resistance can be reduced since the length of the signal, for example signal C, is reduced. The advantage is less power supply voltage drop on the preamp and less power dissipation.

ISSUES

The two issues on appeal are whether Claims 1-6 are anticipated under 35 U.S.C. § 102 by Banouvong and whether or not Claims 1-6 are unpatentable over Contreras in view of Dandia.

GROUPING OF THE CLAIMS

Claim 1 as contained in the attached Appendix is independently patentable, and this rejected claim does not stand or fall together for reasons more clearly set forth herein below.

ARGUMENTS

It is respectfully submitted that Banouvong does not disclose or suggest the presently claimed invention including the communication chip being connected to the head through the first and second rows of connection points.

Banouvong does not relate to read channel technology and does not relate more particularly to a head.

It is respectfully submitted the Contreras does not disclose or suggest the presently claimed invention including the second row of connection points positioned along at least on edge of the communication circuit or behind the first row and the communication chip being connected to the head through the first and second rows of connection points.

Applicants agree with the Examiner's evidence by page 3 of Final Office Action that Contreras fails to disclose the arrangement of the connection points.

Dandia does not disclose or suggest the presently claimed invention including the communication chip being connected to the head through the first and second rows of connection points.

Dandia does not disclose a read channel system and consequently does not disclose a head.

With the present invention, by using inner and outer rows a communication chip including a head, can be constructed to accommodate either eight channel or four channel without redesign of the metals or layers.

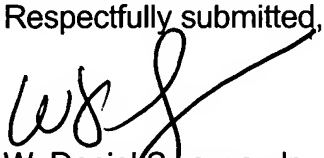
Without a relationship to a head, it is not seen how the above advantages could be achieved from the prior art.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-6 under 35 U.S.C. § 102 and 35 U.S.C. § 103 are not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

Claim 1 (previously presented): A communication chip for a head comprising:

a first row of connection points positioned along at least one edge of said communication chip;

a second row of connection points positioned along at least one edge of said communication chip and behind said first row; and

said communication chip being connected to said head through said first and second rows of connection points.

Claim 2 (previously presented): A communication chip as in Claim 1, wherein said first row of connection points is for a read operation of said head.

Claim 3 (previously presented): A communication chip as in Claim 1, wherein said second row of connection points is for a write operation of said head.

Claim 4 (previously presented): A communication chip as in Claim 1, wherein said first row of connection points is for a write operation of said head.

Claim 5 (previously presented): A communication chip as in Claim 1, wherein said second row of connection points is for a read operation of said head.

Claim 6 (previously presented): A communication chip as in Claim 1, wherein said first row and said second row extend along two sides of said communication circuit.